1,048,576 WORD X 2 BANK X 8 BIT /2,097,152 WORD X 2 BANK X 4 BIT SYNCHRONOUS DRAM

Description

TC59S1608FT is a CMOS synchronous dynamic random access memory organized as 1,048,576-words x2-banks x8-bits and TC59S1604FT organized as 2,097,152 words x2-banks x4-bits. Fully synchronous operations are referenced at the positive edges of clock input and can transfer data up to 100M - bytes per second. These devices are controlled by command setting. Each bank is kept active so that DRAM core sense amplifiers can be used as a cache. The refresh functions, either AutoRefresh or SelfRefresh are easy to use. By having a programmable Mode register, the system can choose the most suitable modes to maximize its performance. These devices are ideal for main memory in applications such as workstations. All inputs and outputs are fully LVTTL compatible.

Features

- Single power supply of 3.3V±0.3
  - Up to 100MHz clock frequency
- Synchronous operation: All signals referenced to the positive edges of clock
- Organization
  - TC59S1608FT
  - 1,048,576 words x 2 banks x 8 bit
  - TC59S1604FT
  - 2,097,152 words x 2 banks x 4 bit
- Program Mode register
- Auto Refresh and Self Refresh
- 4K Refresh cycles / 64ms
- All inputs and outputs: LVTTL compatible
- Package
  - TC59S1608FT: TSOP44-P-400
  - TC59S1604FT: TSOP44-P-400

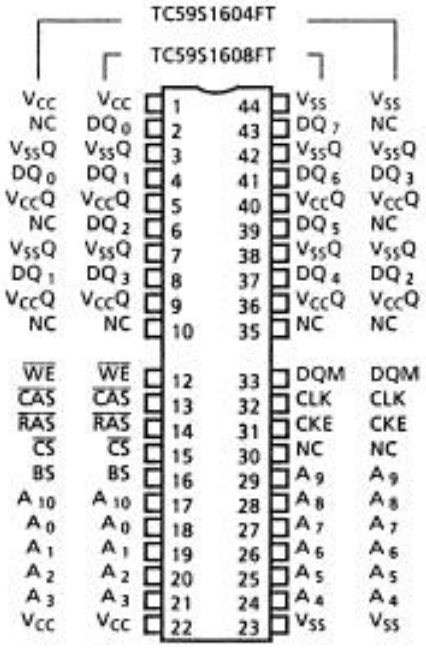
Key Parameters

Item		TC59S1608/1608/1604FT	
		-10	-12
t_{PRD}	Clock Cycle Time (Min.)	10ns	12ns
t_{RAC}	$\overline{RAS}$ Access Time (Max.)	60ns	72ns
t_{CAC}	$\overline{CAS}$ Access Time (Max.)	30ns	36ns
t_{CKA}	CLK Access Time (Max.)	10ns with CL = 3	12ns with CL = 3
t_{RC}	$\overline{RAS}$ Cycle Time (Min.)	100ns	120ns
I_{CC1}	RAS Operation Current (Max.) (Single bank)	80mA	70mA
I_{CC4}	Burst Operation Current (max.)	90mA	80mA
I_{CC7}	Self-Refresh Current (max.)	200µs	200µs

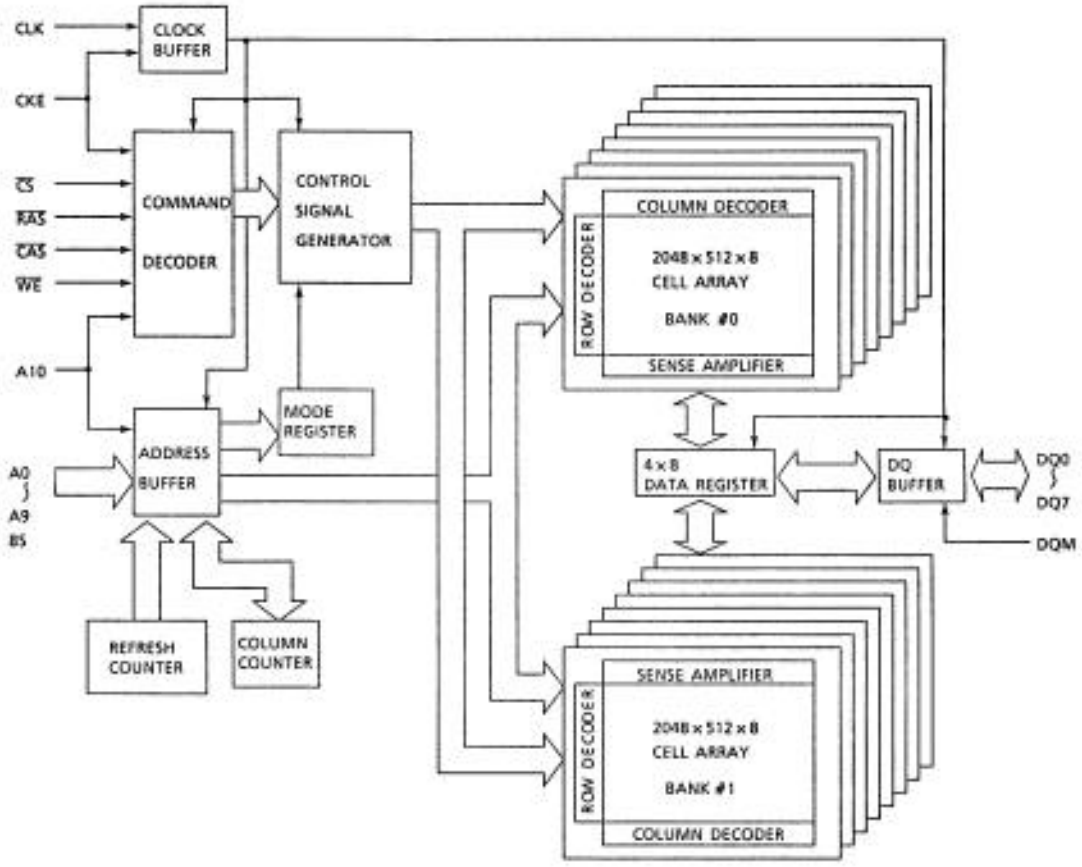
Pin Name

A0~A10	Address
BS	Bank Select
DQ0~DQ7	Data Input/Output
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable Input
DQM	Output disable/ Write Mask
$\overline{CS}$	Chip Select
CLK	Clock inputs
V_{CC}	Power (+3.3V)
V_{SS}	Ground
$V_{CC}Q$	Power (+3.3V) (for I/O buffer)
$V_{SS}Q$	Ground (for I/O buffer)
NC	No Connection

Pin Connection



Block Diagram



Note: This figure is the TC59S1608FT. In the case of TC59S1604FT, the configuration is 2048x1024x4 of cell array and DQ 0-3.

Absolute Maximum Ratings

Symbol	Characteristic	Rating	Unit	Note
V_{IN},V_{OUT}	Input, Output Voltage	-0.5~4.6	V	1
V_{CC}	Power Supply Voltage	-0.5~4.6	V	1
T_{OPR}	Operating Temperature	0~70	°C	1
T_{STG}	Storage Temperature Range	-55~150	°C	1
T_{SOLDER}	Soldering Temperature(10s)	260	°C	1
P_D	Power Dissipation	1	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

Recommended DC Operating Conditions (Ta = 0~70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
V_{CC}	Power Supply Voltage	3.0	3.3	3.6	V	2
$V_{CC}Q$	Power Supply Voltage (for I/O Buffer)	3.0	3.3	3.6	V	2
V_{IH}	Input High Voltage	2.0	-	V_{CC}+0.3	V	2
V_{IL}	Input Low Voltage	-0.3	-	0.8	V	2

Capacitance (V_{CC} = 3.3V ±0.3V, f = 1MHz, Ta = 0~70°C)

Symbol	Parameter	Min.	Max.	Unit
C_I	Input Capacitance	-	4	pF
C_O	Input/Output Capacitance	-	5	

*This parameter is periodically sampled and is not 100% tested.

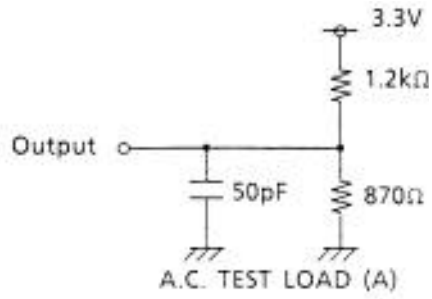
Recommended DC Operating Conditions (V_{CC} = 3.3V ±0.3V, Ta = 0~70°C)

Item		Symbol	-10		-12		Unit	Note
			Min.	Max.	Min.	Max.		
Operating Current t_{PRD}=min, t_{RC} =min Without Burst Operation	1 bank operation	I_{CC1}		80		70	mA	3
	2 bank interleave operation	I_{CC1B}		140		130		
Standby Current t_{PRD}=min, $\overline{CS}$ = V_{IH} $V_{IH/IL}$ = $V_{IH(min)}$/ $V_{IL(max)}$	CKE = V_{IH}	I_{CC2}		7		7	mA	3
	CKE = V_{IL} (Power Down Mode)	I_{CC2PD}		2		2		
Auto Refresh Current t_{PRD}=min, t_{RC} =min Auto Refresh command cycling		I_{CC3}		80		70	mA	3
Burst Operating Current t_{PRD}=min, t_{PC} =min CAS command cycling		I_{CC4}		90		80	mA	3,4
Standby Current t_{PRD}=min, $\overline{CS}$ = V_{IH} $V_{IH/IL}$ = VCC-0.2V/0.2V	CKE = V_{IH}	I_{CC5}		5		5	mA	3,4
	CKE = V_{IL} (Power Down Mode)	I_{CC5PD}		1		1		
No Operating Current t_{PRD}=min CS = V_{IH} bank: active state (2 bank)		ICC6		10		10	mA	3,4
Self Refresh Current Self Refresh mode $\overline{CKE}$ = 0.2V		ICC7		200		200	µA	3,4

Item	Symbol	Min.	Max.	Unit	Note
Input Leakage Current ($0V \le V_{IN} \le V_{CC}$ All other pins not under test = 0V)	$I_{I(L)}$	-5	5	μA	
Output Leakage Current (Output disable, $0V \le V_{IN} \le V_{CCQ}$)	$I_{O(L)}$	-5	5	μA	
Output "H" Level Voltage (I_{OUT} = -2mA)	V_{OH}	2.4	-	V	
Output "L" Level Voltage (I_{OUT} = 2mA)	V_{OL}	-	0.4	V	

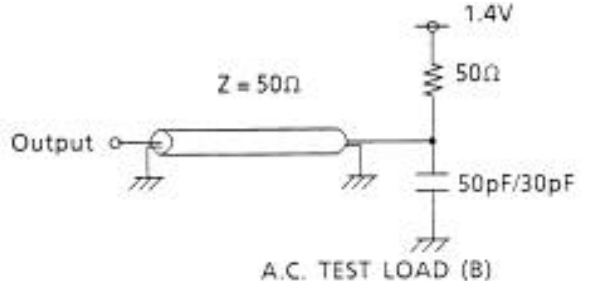
Electrical Characteristics and Recommended AC Operating Conditions (V_{CC} = 3.3V ± 0.3V, Ta = 0~70°C) (Notes 5,6,7)

Symbol	Parameter		-10		-12		Unit	Note
			Min.	Max.	Min.	Max.		
t_{RC}	Random Read or Write Cycle Time		100		120		ns	10
t_{RAC}	Access Time from $\overline{RAS}$			60		72		10
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time		20	30	24	36		10,11
t_{RP}	$\overline{RAS}$ Precharge Time		40		48	-		10
t_{RRD}	$\overline{RAS}$ to $\overline{RAS}$ Delay Time		20		24			10
t_{CAC}	Access Time from $\overline{CAS}$			30		36		
t_{PC}	Page Mode Cycle Time		2		2		Cycle	
t_{RSH}	$\overline{RAS}$ Hold Time		2		2			
t_{WR}	Write Recovery Time		1		1			
t_{CKA}	Access Time from CLK	$\overline{CAS}$ Latency = 2		12.5/11.5		15/14	ns	8
		$\overline{CAS}$ Latency = 3		10/9		12/11		
		$\overline{CAS}$ Latency = 4		10/9		12/11		
t_{RST}	Burst Cycle Reset Time		20		24			10
t_{OH}	Output Data Hold Time		5		6			
t_{OHZ}	Output Data Hold - Impedance Time		5	10	6	12		9
t_{ACT}	Power Down Mode Exit Time		0	15	0	18		
t_{SB}	Power Down Mode Entry Time		0	15	0	18		
t_{RAS}	$\overline{RAS}$ to Precharge Command Delay Time		60	100000	72	100000		10
t_{STUP}	Input Data Set-up Time		2		2			
t_{HOLD}	Input Data Hold		3		4			
t_T	Transition Time of CLK (Rise and Fall)		1	10	1	10		
t_{PRD}	CLK Cycle Time		10	1000	12	1000		
t_{CLKH}	CLK High Level Width		2		3			12
t_{CLKL}	CLK Low Level Width		2		3			12
t_{REF}	Refresh Period			64		64	ms	
t_{RSC}	Mode Register Set Cycle Time		40		48		ns	10
t_{RH}	Register Set Data Hold Time		8		10			
t_{RS}	Register Set Data Set-up Time		2		2			
t_{OLZ}	Output Data Low Impedance		0		0			



AC Test Conditions

Reference Level of Output Signals	1.4V/1.4V
Output Load	Reference to the Under Output Load
Input Signal Levels	2.0V/0.8V
Transition Time (Rise and Fall) of Input Signals	2ns
Reference Level of Input Signals	1.4V



NOTE:

1. Stresses greater than those listed under “Absolute Maximum Ratings “may cause permanent damage to the device.
2. All voltage are referenced to V_{SS}.
3. These parameters depends on the cycle rate and these values are measured by the cycle rate under the minimum value of t_{PRD} and t_{RC}.
4. These parameters depends on the output loading. Specified values are obtained with the output open.
5. Power must be turned on in the following sequence.
   (1) Apply power and start clock.
   During V_{CC} ramping up to the valid level, DQM and CKE should be the same as V_{CC} to ensure output Hi-z.
   (2) Maintain stable power, stable clock, and NOP input condition for a minimum of 200 μs.
   (3) Issue precharge command to all banks of the device.
   (4) Issue a mode register set command to initialize the mode register.
   (5) Issue 8 or more autorefresh commands.
6. A.C. measurements assume t_T=2ns.
7. 1.4V is the reference level for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}. Transition (rise and fall) of input signals are fixed slope.
8. Output data reference levels: 1.4V/ 1.4V
9. t_{OD}(max.) defines the time at which the outputs achieve the open circuit condition and are not reference levels.
10. These parameters account for the number of clock cycle and depend on the operating frequency of the clock, as follows: the number of clock cycles = specified value of timing / clock period (count fractions as a whole number).

Latency relationship to frequency (Unit: clock cycles)

TC59S1608FT-10 (Calculation with t_{PRD} = 10ns~30ns)

clock period (t_{PRD})	t_{RC}	t_{RP}	t_{RRD}	t_{CAC}	t_{RAS}	t_{RAC}	t_{RSC}	t_{RST}
	100ns	**40ns**	**20ns**	**30ns**	**60ns**	**60ns**	**40ns**	**20ns**
≥30ns	4	2	1	2	2	2	2	1
≥20ns	5	2	1	2	3	3	2	1
≥20ns	7	3	2	2	4	4	3	2
≥13ns	8	3	2	3	5	5	3	2
≥12ns	9	4	2	3	5	5	4	2
≥10ns	10	4	2	3	6	6	4	2

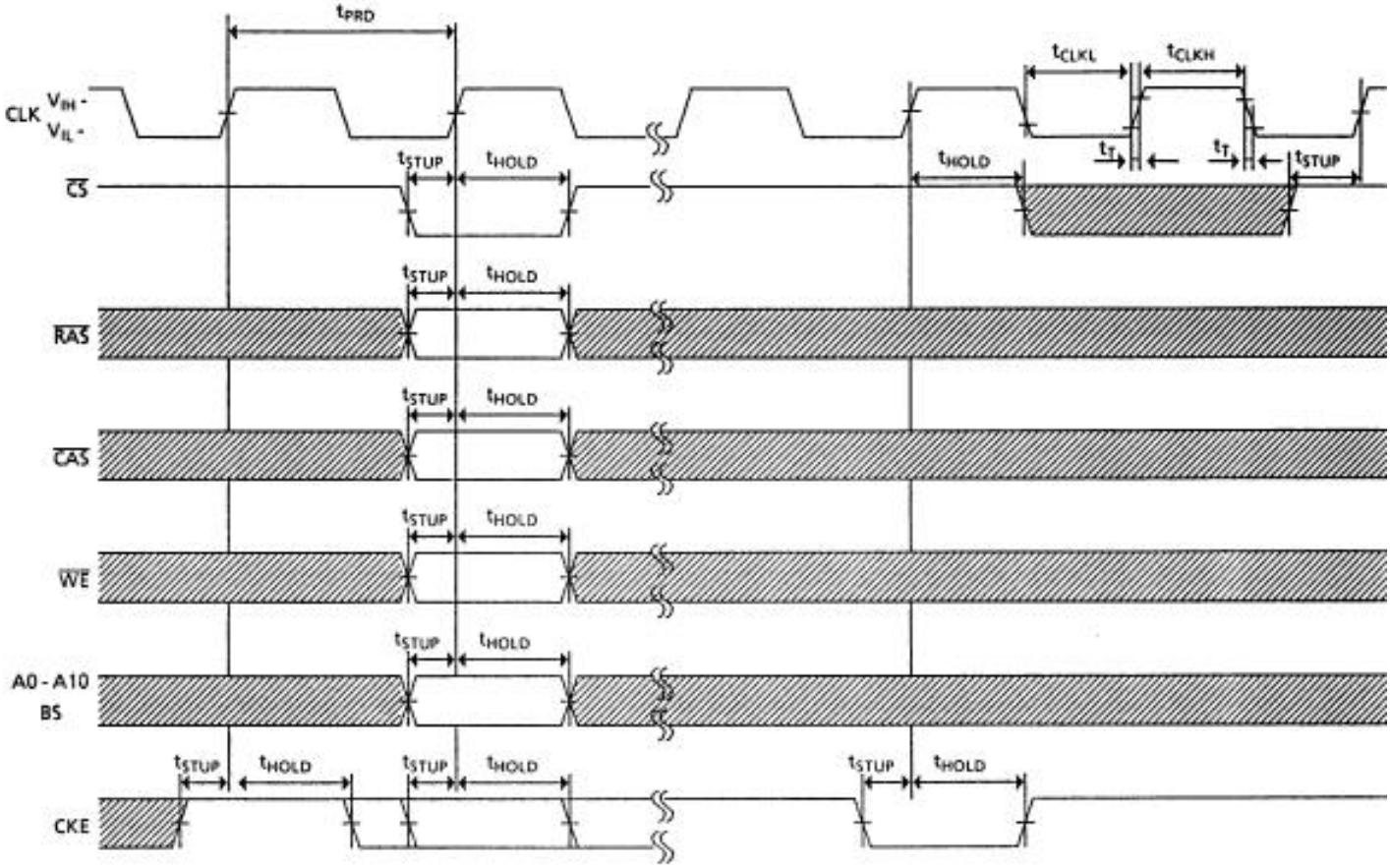
TC59S1608FT-12 (Calculation with t_{PRD} = 12ns~30ns)

clock period (t_{PRD})	t_{RC}	t_{RP}	t_{RRD}	t_{CAC}	t_{RAS}	t_{RAC}	t_{RSC}	t_{RST}
	120ns	**48ns**	**24ns**	**36ns**	**72ns**	**72ns**	**48ns**	**24ns**
≥24ns	5	2	1	2	3	3	2	1
≥18ns	7	3	2	2	4	4	3	2
≥16ns	8	3	2	3	5	5	3	2
≥14.4ns	9	4	2	3	5	5	4	2
≥12ns	10	4	2	3	6	6	4	2

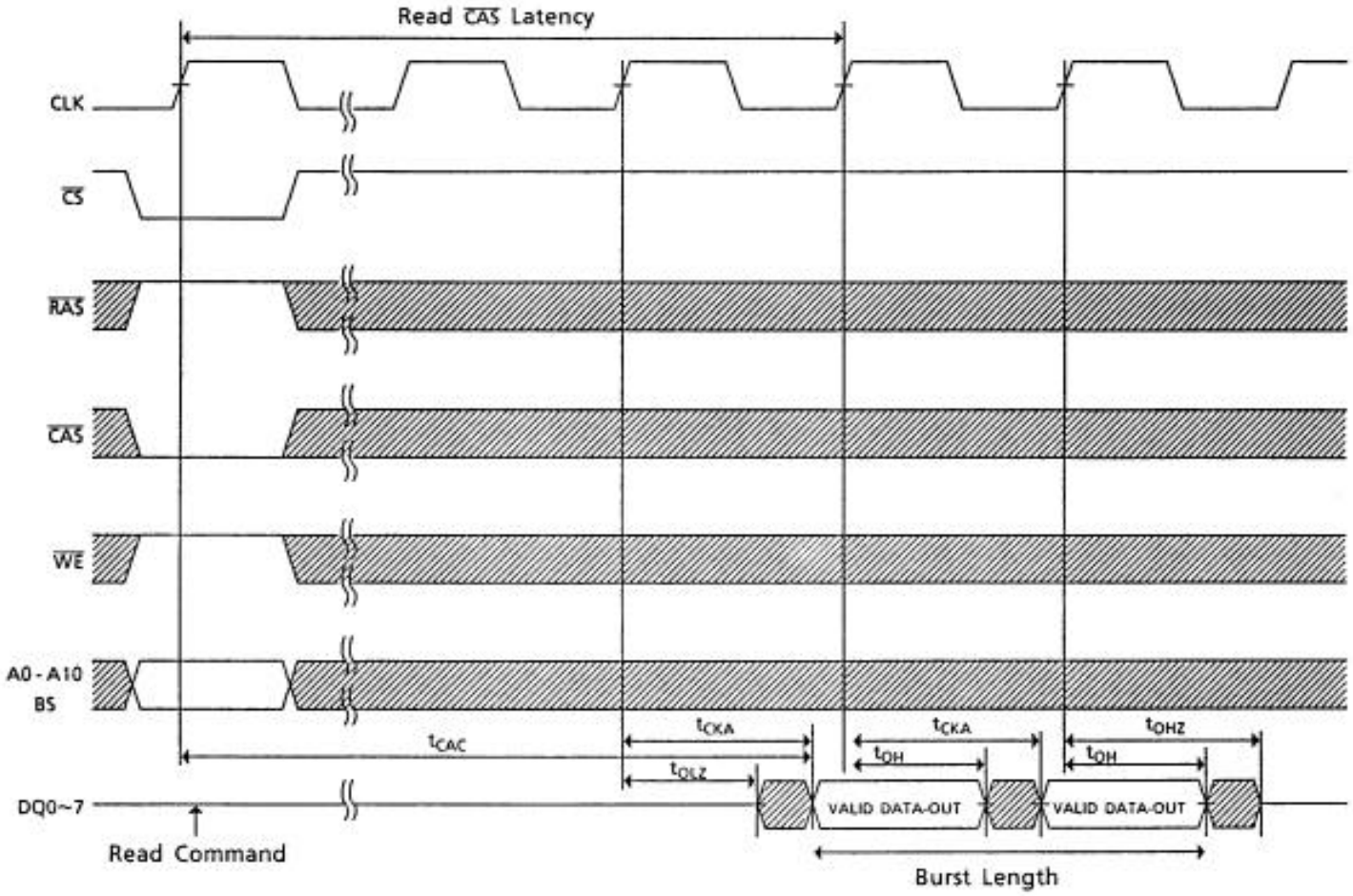
11. The value of t_{RCD}(max.) guarantees t_{RAC}(max.) and doesn't specify the operating limit.When t_{RCD} is longer than t_{RCD} (max.) in a read cycle, the access time is specified by t_{CAC}. Also, when t_{RCD} is shorter than t_{RCD} (max.) in a read cycle, the access time is specified by t_{RAC}. Therefore, Read CAS Latency field in the Mode register must specify the value of t_{CAC} = t_{RAC} - t_{RCD} in clock cycle.
12. t_{CLKH} is the pulse width of CLK measured from the positive edge to the negative edge referenced to V_{IH} (min.). t_{CLKL} is the pulse width of CLK measured from the negative edge to the positive edge referenced to V_{IL}(max.).

Timing Waveform

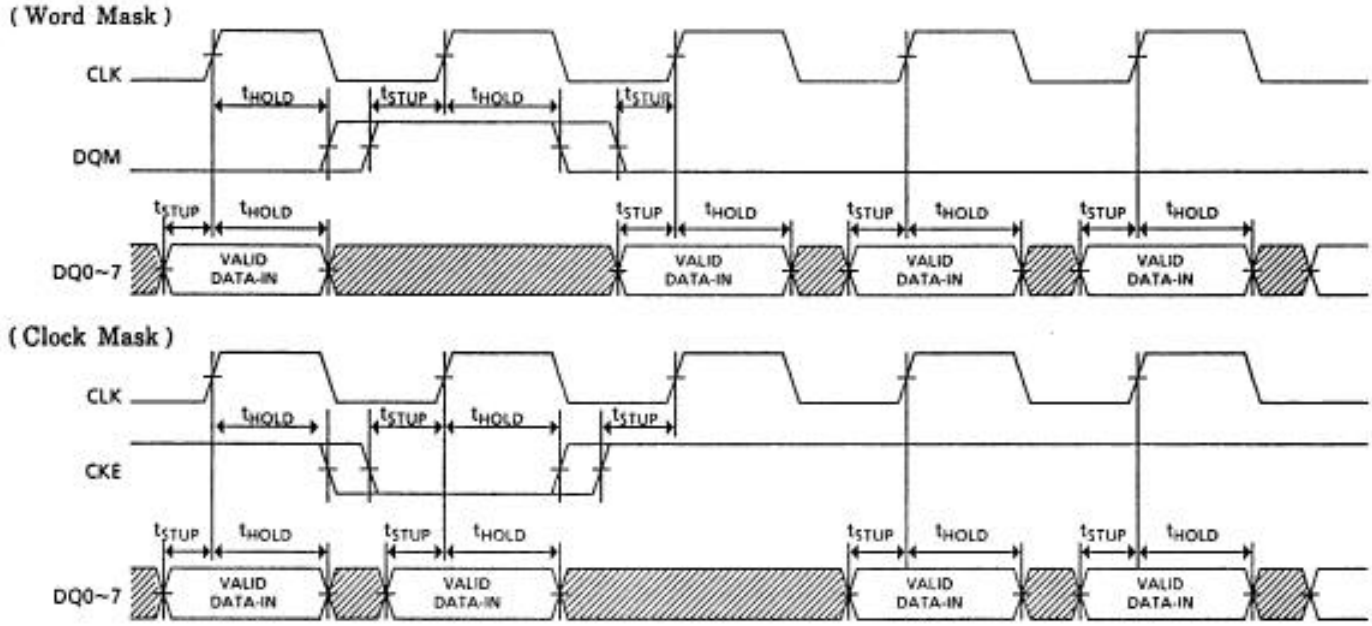
Command Input Timing



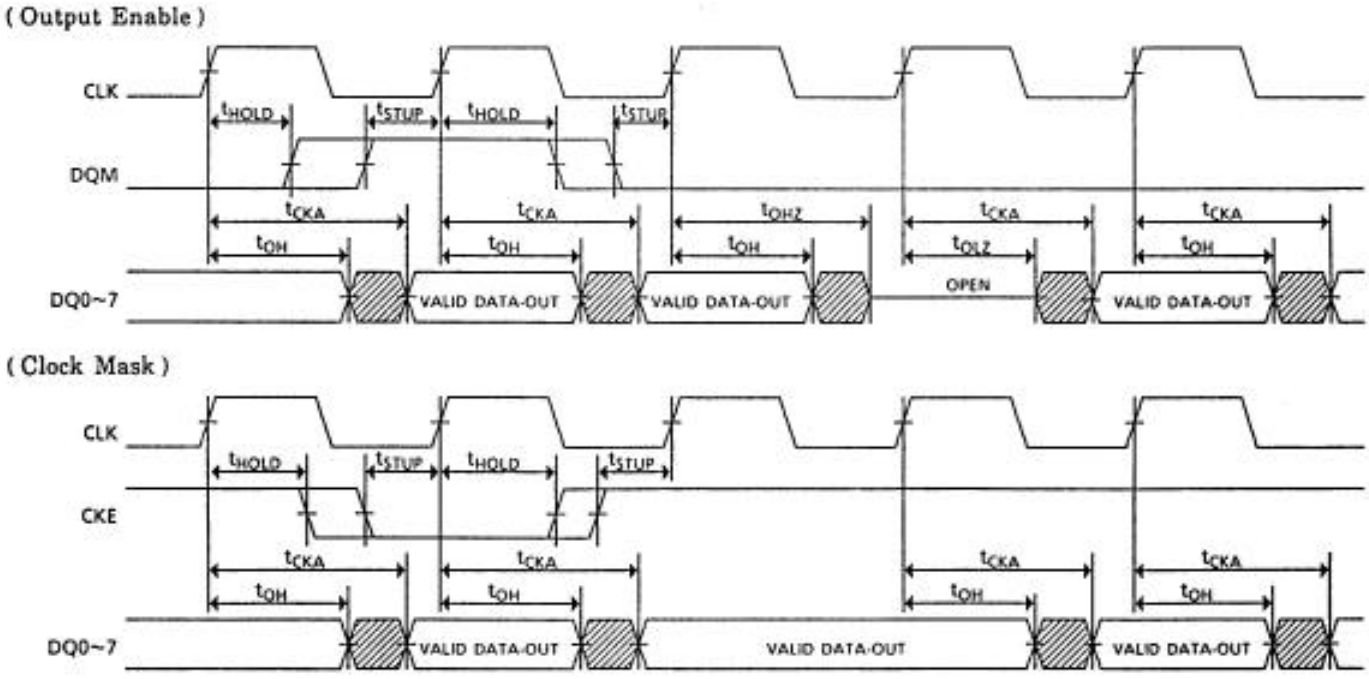
Read Timing


Read CAS Latency
CLK
CS
RAS
CAS
WE
A0 - A10
BS
DQ0~7
tCAC
tCKA
tOLZ
tCKA
tOH
tOHZ
tOH
VALID DATA-OUT
VALID DATA-OUT
Read Command
Burst Length

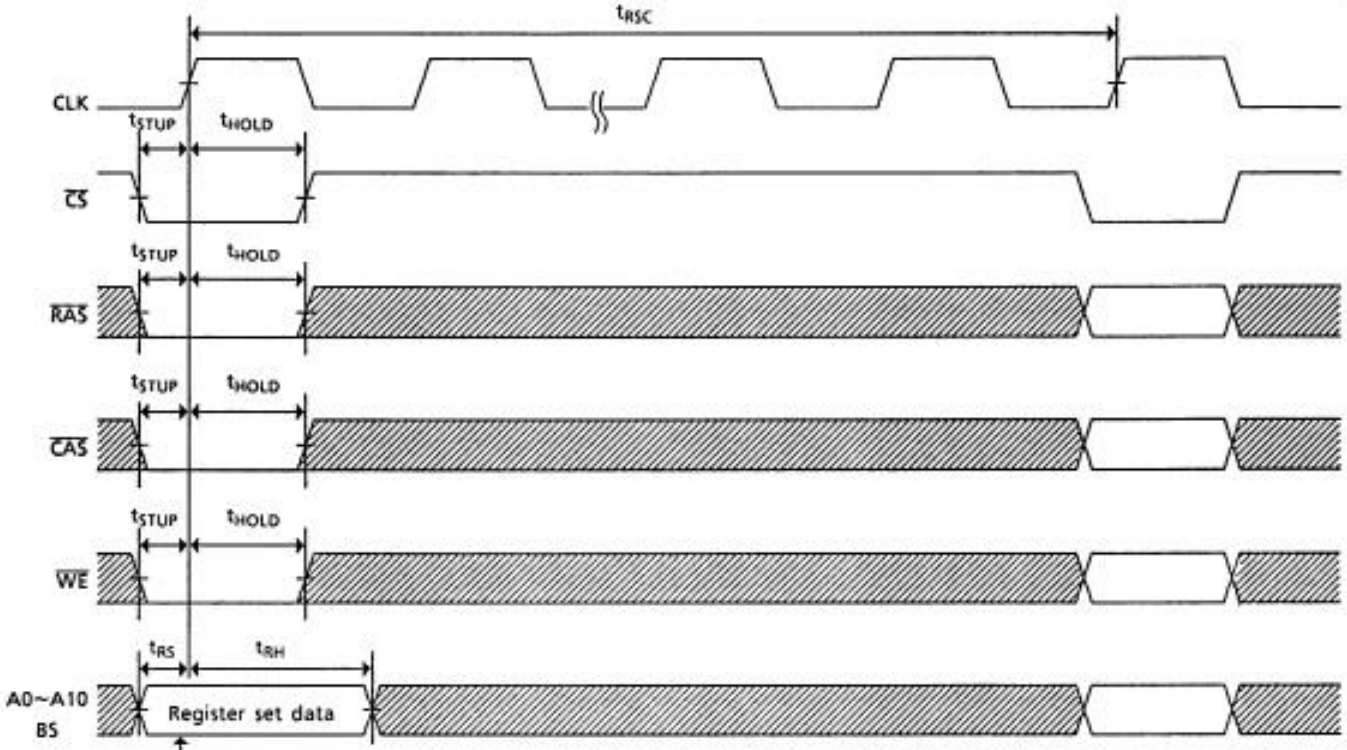
Control Timing of Input Data



Control Timing of Output Data



Mode Register Set Cycle



A0	Burst Length	
A1		
A2		
A3	Addressing Mode	
A4	$\overline{CAS}$ Latency	
A5		
A6		
A7	"0"	(Test Mode)
A8	"0"	Reserved
A9	"0"	
A10	"0"	
BS	"0"	

			Burst Length	
A2	A1	A0	Sequential	Interleave
0	0	0	Reserved	Reserved
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1		
1	1	0		
1	1	1		

A3	Addressing Mode
0	Sequential
1	Interleave

A6	A5	A4	$\overline{CAS}$ Latency
0	0	0	Reserved
0	0	1	
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	Reserved
1	1	0	
1	1	1	

Operating Timing Example

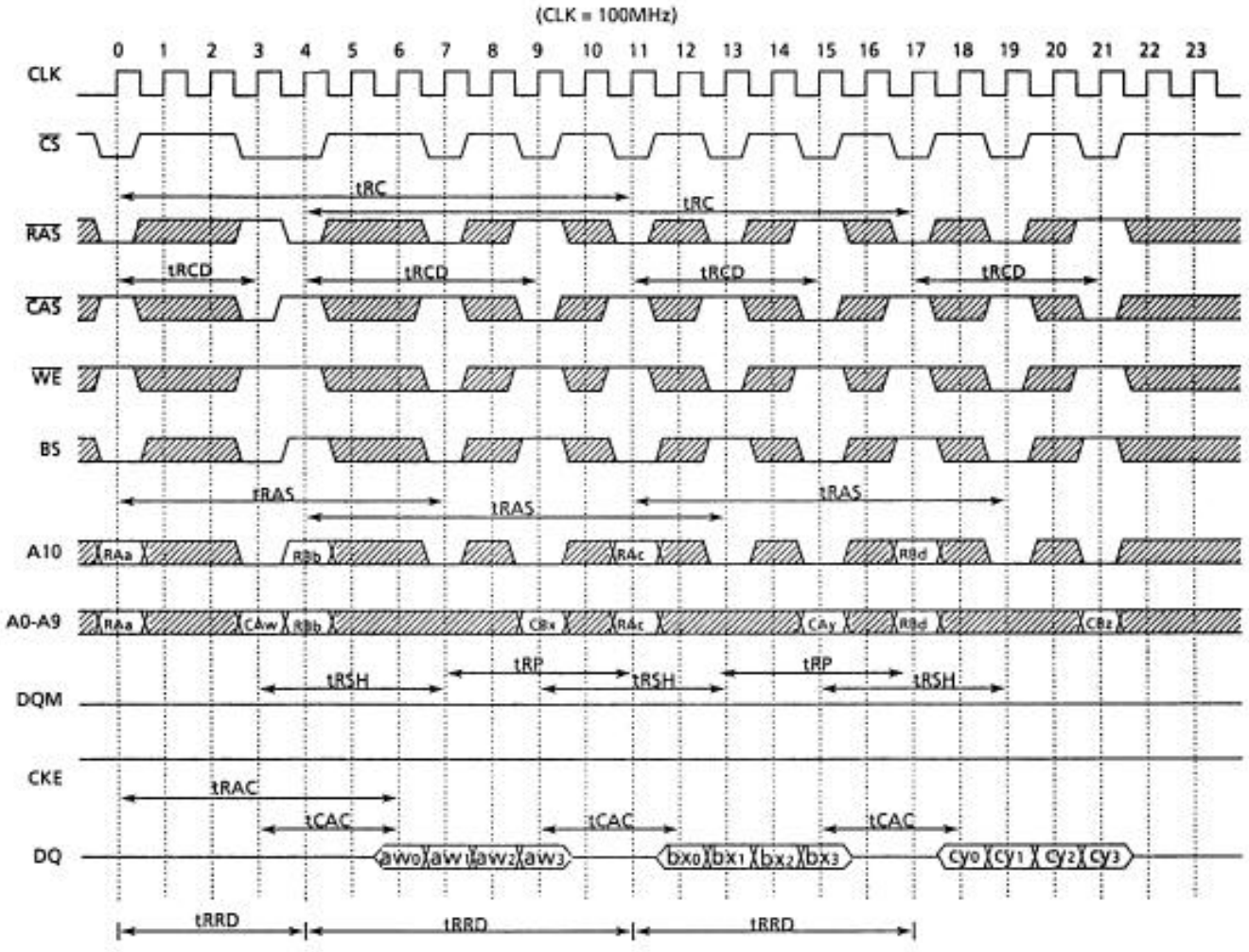


Figure 1. Interleaved Bank Read (Burst Length = 4, $\overline{\text{CAS}}$ Latency = 3)

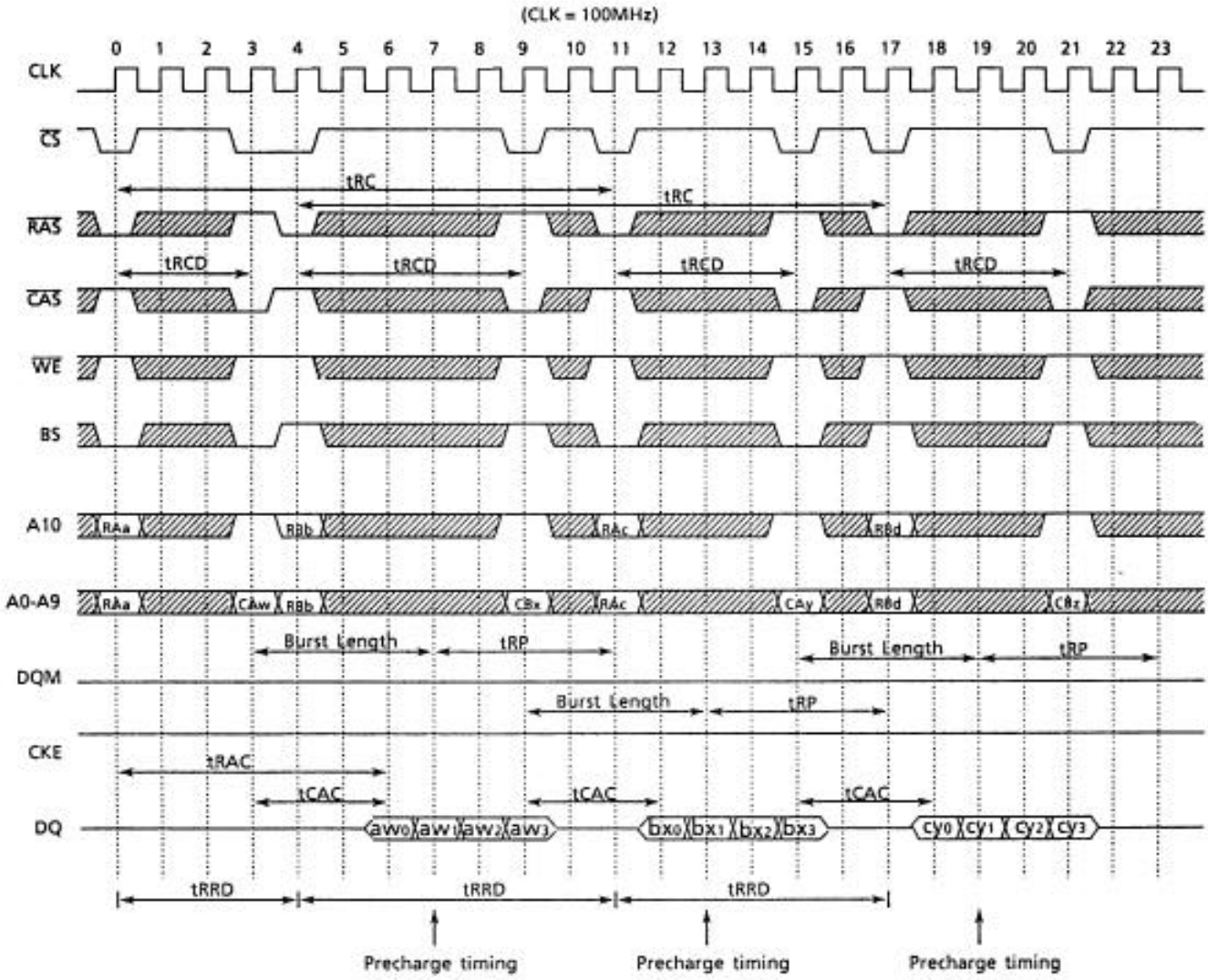


Figure 2. Interleaved Bank Read (Burst Length = 4, $\overline{\text{CAS}}$ Latency = 3, Autoprecharge)

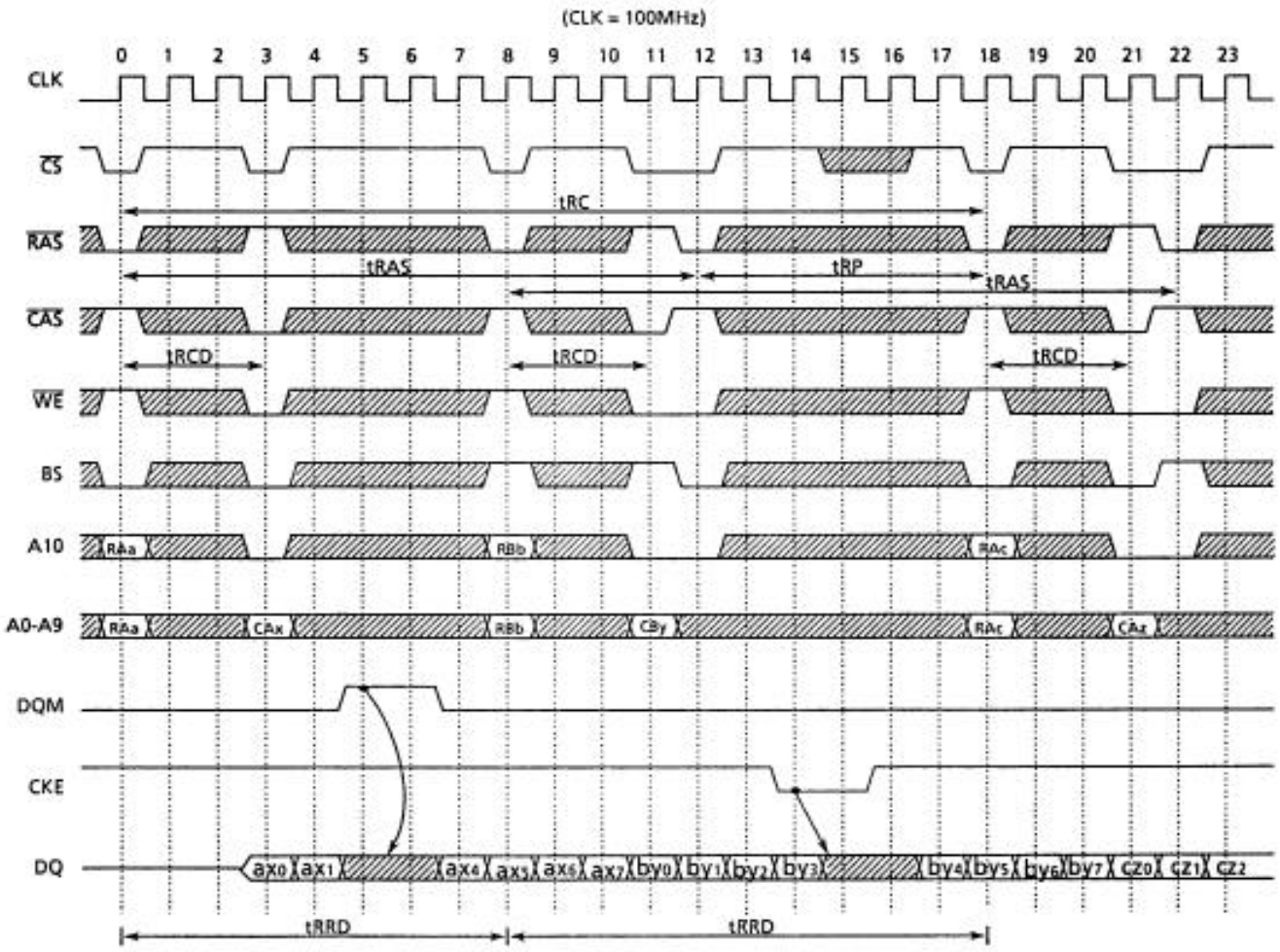


Figure 3. Interleaved Bank Read (Burst Length = 8, $\overline{\text{CAS}}$ Latency = 3)